## REMARKS

This is a full and timely response to the outstanding final Office action mailed on July 11, 2008. Reconsideration and allowance of the application and presently pending claims 6-10 are respectfully requested.

### Present Status of the Application

In the outstanding final Office action, the specification and abstract of the present invention are objected to because of informalities. Examiner indicates Applicant to correct the informalities in the specification and abstract of the present invention, and further requests the Applicant's cooperation in correcting any errors of which applicant may become aware in the specification.

Claim 1 is objected to because of informalities.

Claims 1 and 3 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Claims 2, 4, and 5 are rejected under 35 U.S.C. 112, first paragraph as being dependent upon the rejected base claims. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai (US 2004/0075636 A1, hereinafter referred to as "Pai") in view of Sunohara (US 2003/0038771 A1, hereinafter referred to as "Sunohara"). Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pai and Sunohara as applied to claim 1 above, and further in view of Chow (US 6,836,149 B2, hereinafter referred to as "Chow").

Claim 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai and Sunohara as applied to claim 3 above, and further in view of Matsuura (US 5,619,169, A hereinafter referred to as "Matsuura").

Responsive thereto, Applicant has corrected the abstract and specification of the present invention, and objections to the abstract and specification of the present invention are solicited respectfully. Claims 1-5 are cancelled, and claims 6-10 are added. Allowance of claims 6-10 is courteously requested.

**Amendments of the Specification and the Abstract**

Referring to the new filed specification with remarks, the amendments in the specification can be indicated in the new specification with remarks. Applicant amends the informalities and grammar errors that Examiner indicates, and Applicant finds by his self. Furthermore, Applicant further amends the errors in translation, and the correct translated specification is submitted and filed with this response. Therefore, it is believed no new matter is introduced. The amendments for being entered are courteously requested.

**Newly Added Claims**

Responsive thereto, Applicant has cancelled claims 1-5 and added claims 6-10. Claims 6-10 are supported by the original figures and specification of the present invention, and the reasons thereof are described in the following description. Claims 6-10 are can overcome the combination of the cited references, however, Applicant knows Examiner must search new references and reconsider. If there is no prior art disclosing,

teaching, or implying the features in claims 6-10, claims 6-10 will be patentable.

Claim 6 is recited as follows:

"6. A cascade driving circuit, suitable for a liquid crystal display (LCD), comprising:

a first driving circuit unit, for receiving a differential input signal and generating a first differential data signal for driving the LCD, and a first differential output signal; and

a second driving circuit unit, coupled to the first driving circuit unit, for receiving the first differential output signal and generating a second data signal for driving the LCD;

wherein **the differential input signal is amplified for a first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level, and the first predetermined period is less than a first period of the differential input signal being in a steady state.**" **(Emphasis Added)**

Referring to FIG. 2 of the present invention, it shows a cascade driving circuit for driving an LCD. It disclose the cascade driving circuit has a first driving circuit unit (the first 220) and a second driving circuit unit (the second 220). The first driving circuit unit receives a differential input signal (output of 240) and generates a first differential data signal (222 of the first 220) for driving the LCD (210), and a first differential output signal (224 of the first 220). The second driving circuit unit is coupled to the first driving circuit unit, and used to receives the first differential output signal (224 of the first 220) and generates a second data signal (220 of the second 220) for driving the LCD.

It is obvious that FIG. 2 does not disclose the features, "the differential input signal is amplified for a first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level, and the first predetermined period is less than a first period of the differential input signal being in a steady state". Referring to FIG. 7, it shows the differential input signal (720) is amplified for a first predetermined period (the period that the level of 730 is in the range of the first lowest and second lowest, or the period that the level of 730 is in the range of the first highest and second highest) when the differential input signal changes from a high level to a low level (720 changes from the high level to the low level), or from the low level to the high level (720 changes from the low level to the high level), and the first predetermined period is less than a first period of the differential input signal being in a steady state (the period that 720 maintains low or high). Therefore, claim 6 is supported by the original specification, and it is believed no new matter is introduced.

The cited references do not disclose, teach, or imply the features, "the differential input signal is amplified for a first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level, and the first predetermined period is less than a first period of the differential input signal being in a steady state", and therefore claim 6 overcomes the cited references. However, Applicant knows Examiner must search new references and reconsider. If there is no prior art disclosing, teaching, or implying the features in claim 6, claim 6 will be patentable.

Furthermore, the features "the differential input signal is amplified for a first predetermined period when the differential input signal changes from a high level to a

low level, or from the low level to the high level, and the first predetermined period is less than a first period of the differential input signal being in a steady state", may generate an unexpected result. Referring to FIG. 3 of the present invention, during the signal transmission, the signal attenuation may seriously affect the performance of the conventional cascade driving circuit. Though amplification may compensate the signal attenuation, it may induce large power consumption. By contrast, in the present invention, the differential input signal is amplified for a first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level, and the first predetermined period is less than a first period of the differential input signal being in a steady state. Therefore, the cascade driving circuit in claim 6 can compensate the signal attenuation and reduce the power consumption. It is noted that, the amplification is performed when the differential input signal changes from a high level to a low level, or from the low level to the high level. That is because during the signal transmission, the transition state of the signal may be affected seriously. Therefore, in order to reduce the power consumption and compensate the signal attenuation, the amplification is performed when the differential input signal changes from a high level to a low level, or from the low level to the high level.

Claim 10 depends on claim 6, and is supported by the original specification. Claim 10 is a cascade driving circuit with three stages, which can be supported by FIG. 2 of the present invention, and therefore no new matter is introduced. If claim 6 is patentable, claim 10 will be also patentable as matter of law.

Referring to FIG. 6 of the present invention, the first driving circuit (610) comprises first differential receiver (620), a first differential transmitter (630), and a first

differential signal amplifier (640). Therefore, claim 7 is supported by FIG. 6 of the present invention, and therefore no new matter is introduced. If claim 6 is patentable, claim 7 will be also patentable as matter of law.

Claim 8 describes the structure of the first differential transmitter. Referring to FIG. 5 of the present invention, the first differential transmitter (501) comprises a first current source (510), a first transistor (520), a second transistor (530), a third transistor (540), and a fourth transistor (550). A drain of the first transistor and a drain of the second transistor are coupled to the first current source, a source of the first transistor is coupled to a drain of the third transistor and a negative input end (522) of the first differential signal amplifier. Gates of the second and third transistors are coupled to a positive output end (the "+" in FIG. 5) of the first differential receiver, and a source of the second transistor is coupled to a drain of the fourth transistor and a positive input end (532) of the first differential signal amplifier. Sources of the third and the fourth transistors are coupled to a ground voltage, and gates of the first and fourth transistors are coupled to a negative output end (the "-" in FIG. 5) of the first differential receiver.

Claim 8 is supported by FIG.5 of the present invention, and it is believed no new matter is introduced. Claim 8 depends on claim 6, and if claim 6 is patentable, claim 8 will be patentable as matter of law.

Claim 9 describes the structure of the first differential signal amplifier. Referring to FIG. 8 of the present invention, the first differential signal amplifier comprises a second current source (810), a third current source (820), a first resistor (870), a second resistor (820), a first sensor switch (830), a second sensor switch (840), a third sensor switch (850), and fourth sensor switch (860). A second terminal of the

first resistor and a second terminal of the second resistor are coupled to a ground voltage. A first terminal of the first sensor switch and a first terminal of the second sensor switch are coupled to the second current source, and a first terminal of the third sensor switch and a first terminal of the fourth sensor switch are coupled to the third current source. A second terminal of the first sensor switch and a second terminal of the third sensor switch are coupled to a first terminal of the first resistor, a positive out end (Tx+) of the first differential transmitter, and a positive output end (Tx+) of the first differential signal amplifier. A second terminal of the second sensor switch and a second terminal of the fourth sensor switch are coupled to the a first terminal of the second resistor, a negative out end (Tx-) of the first differential transmitter, and a negative output end (Tx-) of the first differential signal amplifier. The first, second, third, and fourth sensor switches are controlled by whether the input differential signal changes from the high level to the low level, or from the low level to the high level, or the input differential signal is in the steady state (see FIG. 7 and paragraphs [0031-0032]).

Claim 9 is supported by the figures and specification of the present invention, and it is believed no new matter is introduced. Claim 9 depends on claim 6, and if claim 6 is patentable, claim 9 will be patentable as matter of law.

Accordingly, allowance and reconsideration of added claims 6-10 are requested respectfully.

## CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 6-10 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Nov. 11, 2008

Belinda Lee

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw